MODULE-1 TRANSISTOR BIASING

BIPOLAR JUNCTION TRANSISTOR

Introduction

TRANS / ISTOR

Transfer of Resistance

Transistor transfers the signal from one resistance level to another resistance level i.e. signal transferred from i/p port to o/p port.

(or)

while transfering the signal from i/p port to o/p port it does the amplification process.

Depending on conduction of current due to charged particles (e^- & holes) transistors are classified into:

1. Bipolar transistor
2. Unipolar transistor

1. Bipolar transistor:

The current conduction due to both e^- & holes.

Ex:- BJT

Depending on construction principle BJT classified into

1. NPN transistor
2. PNP transistor

(*) BJT is a current controlled device i.e., the o/p current is controlled by the i/p current.

2. Unipolar transistor :-

The current conduction due to either e^- (or) holes.

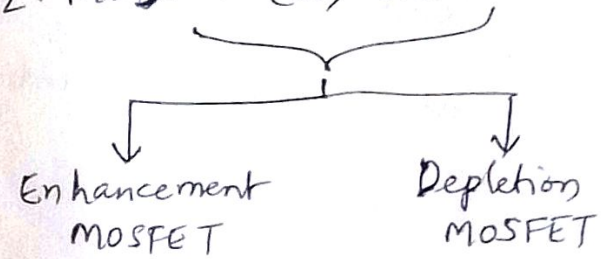
EX :- FET.

The current conduction due to only e^- – N channel

The current conduction due to only holes – P channel

Depending on the constraction principle FETs are classified into :

1. JFET
2. MOSFET (or) Insulated gate FET (IGFET)

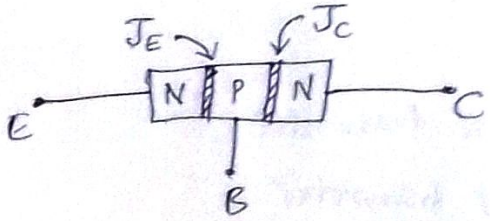


(*) FET is a voltage controlled device.

i.e. the o/p current is controlled by the i/p voltage.

(*) Bipolar Junction transistor (BJT) :-

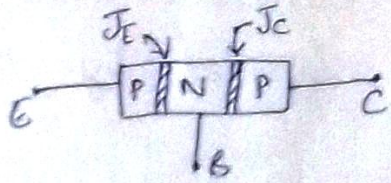
NPN transistor :-



J_E → Emitter-base Junction

J_C → Collector-base Junction

PNP transistor :-



Emitter :- Emits the charged particles
- Heavily doped.
- Medium in size.

Collector :- Collects the charged particles emitted by emitter
- Moderately doped.
- Large in size.

Base :- Controls the current through the transistor.
- Lightly doped.
- Small in size.

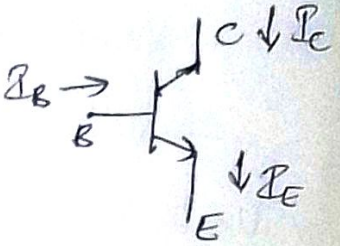
* The main purpose of transistor is amplification.
To do this, the transistor must be properly biased.
(i.e. forward biased (F.B.) or reverse biased (R.B.))

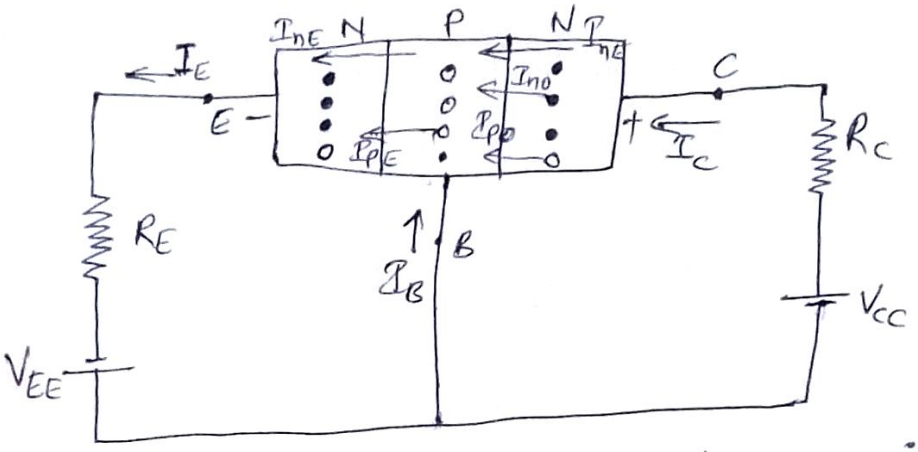
Ex:- J_E – F.B. } → Active region.
J_C – R.B. }

Junctions	Region of operation	Application
J_E – R.B. J_C – R.B.	Cut off region	→ OFF switch
J_E – F.B. J_C – R.B.	Active region	→ Amplifier
J_E – F.B. J_C – F.B.	Saturation	→ ON switch
J_E – R.B. J_C – F.B.	Inverse active region ↓ (Not economical, so it is never used)	→ Attenuator ↓ (reduce the amplification)

* Transistor current components

$$I_E = I_C + I_B \quad \rightarrow (1)$$





I_{nE} → current due to e^- [which are majority carriers in emitter E region)

I_{pE} → current due to holes [which are majority carriers of base flowing into 'E' region)

I_{no} → current due to e^- [which are minority carriers of base flowing from 'c' region).

I_{po} → current due to holes [which are minority carriers of 'C' flowing from 'C' to 'B']

I_{nC} → current due to e^- [due to collection of e^- by the collector from the emitter]

$$\therefore I_{nE} > I_{nC}$$

$$I_E = I_{nE} + I_{pE} \quad \rightarrow (2)$$

$$I_C = I_{nC} + I_o \quad \rightarrow (3)$$

where $$I_o = I_{no} + I_{po} \quad \rightarrow (4)$$

Equations (1) to (4) are called transistor fundamental current equations.

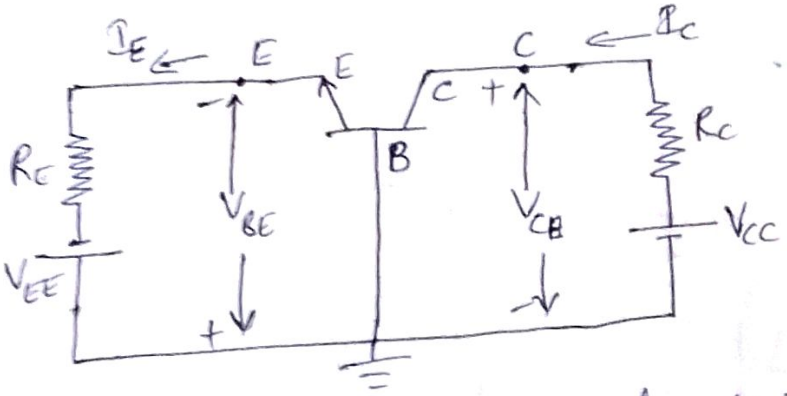
In transistor acting as an amplifier,

current gain (α) [Common Base]:-

$$\alpha = \frac{\text{The injected majority carrier current at 'C'}}{\text{Total emitter current.}}$$

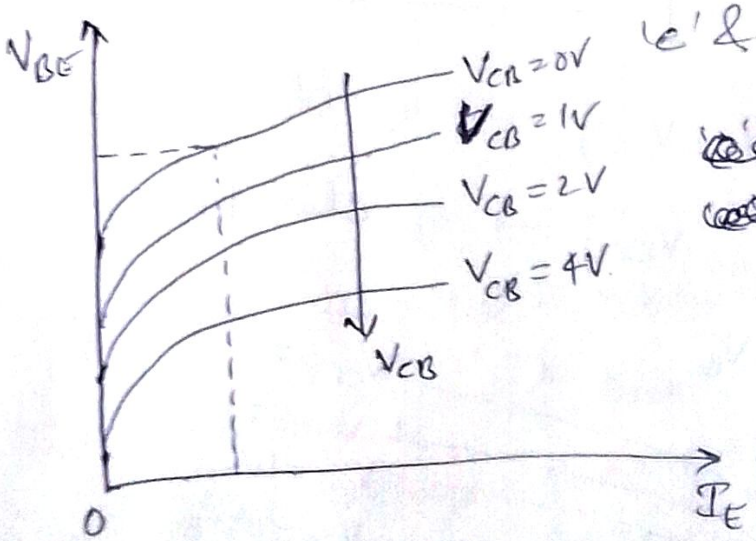
'β' is current gain in CE configuration.
'γ' is current gain in CC configuration.

(*) Common Base characteristics:-



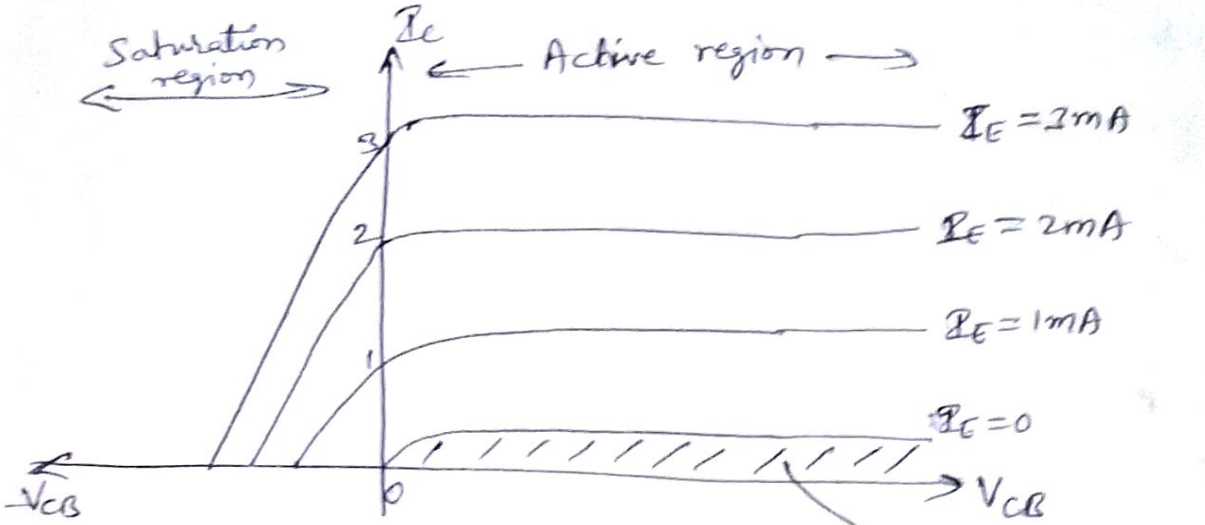
$V_{BE} = f[I_E, V_{CB}]$ → i/p characteristics

$I_C = f[I_E, V_{CB}]$ → o/p characteristics.



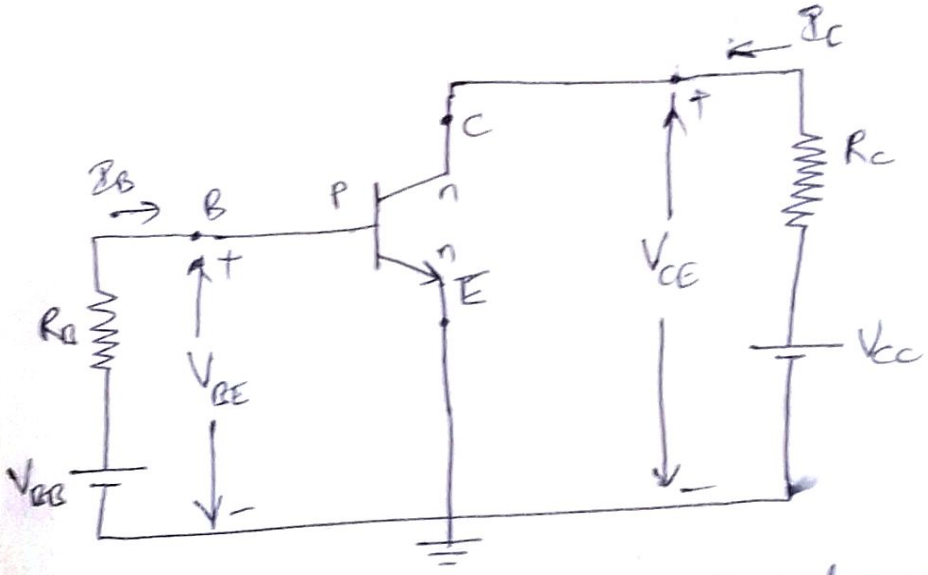
'e' & 'b' → short-circuited

i/p characteristics



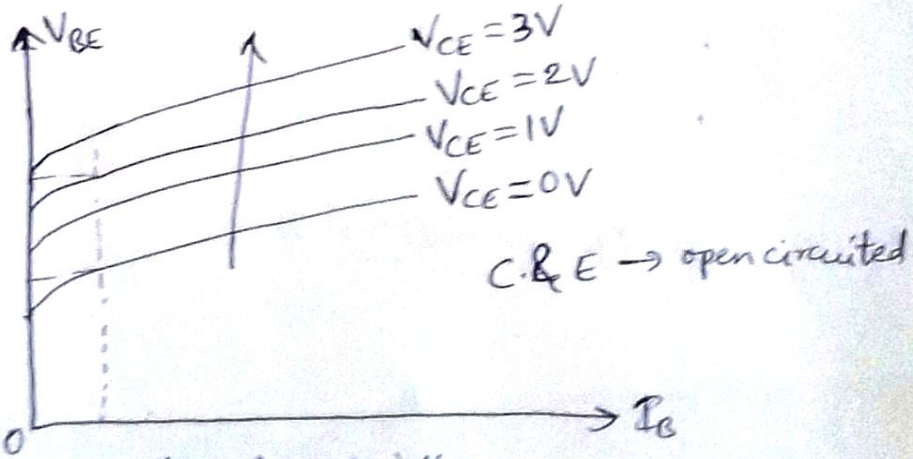
o/p characteristics

(*) Common Emitter characteristics :-

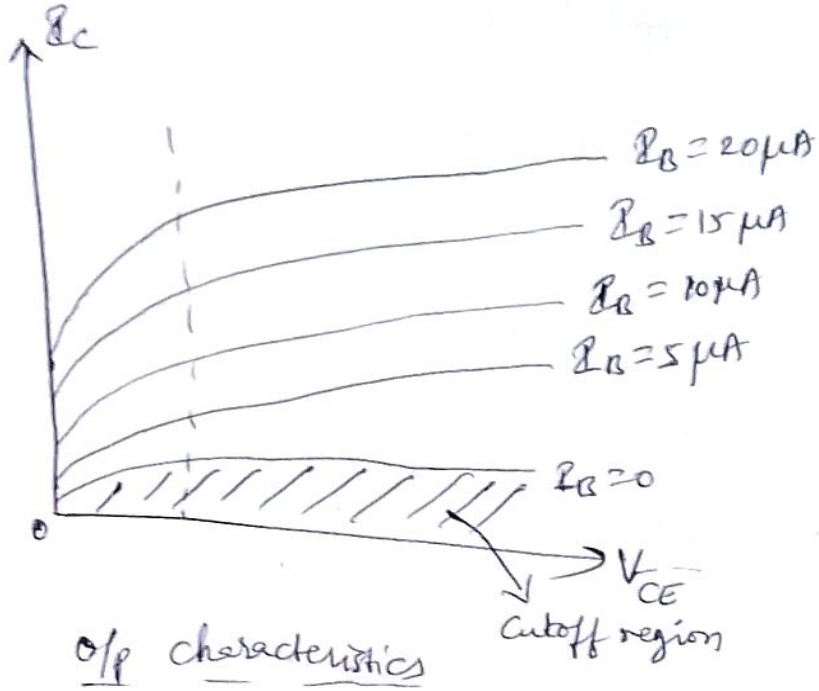


$V_{BE} = f[I_B, V_{CE}]$ → i/p characteristics

$I_C = f[I_B, V_{CE}]$ → o/p characteristics



i/p characteristics



O/p characteristics

The common collector characteristics are similar to common emitter characteristics.

The i/p characteristics V_{BE} replaced by V_{CB} & the O/p characteristics I_C replaced by I_E.

(*) Relation between α & β :-

$$\alpha = \frac{\beta}{1+\beta}$$

(or)

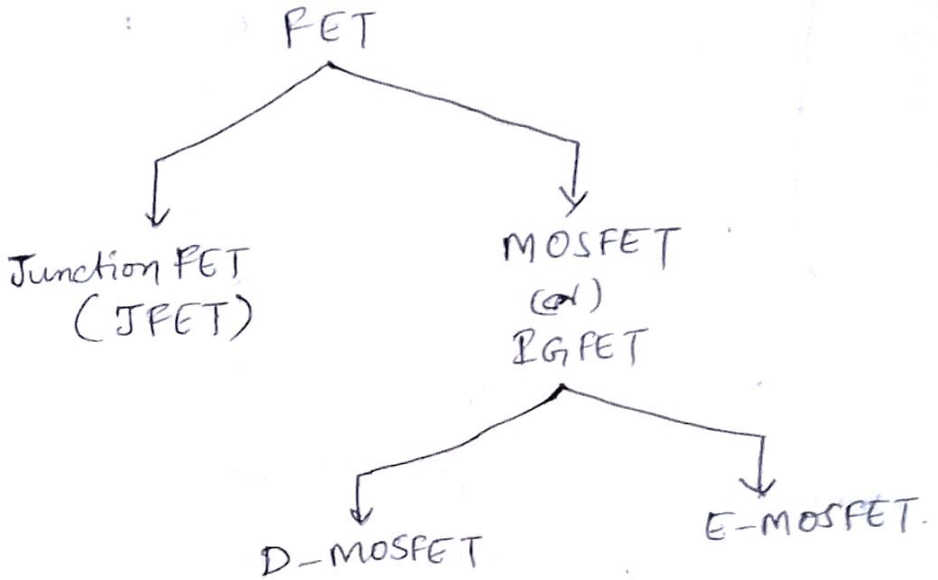
$$\beta = \frac{\alpha}{1-\alpha}$$

(*) Early Effect (or) Base width modulation :-

The variation of the base width in accordance with the applied voltage across the collector junction is called base width modulation (or) Early Effect.

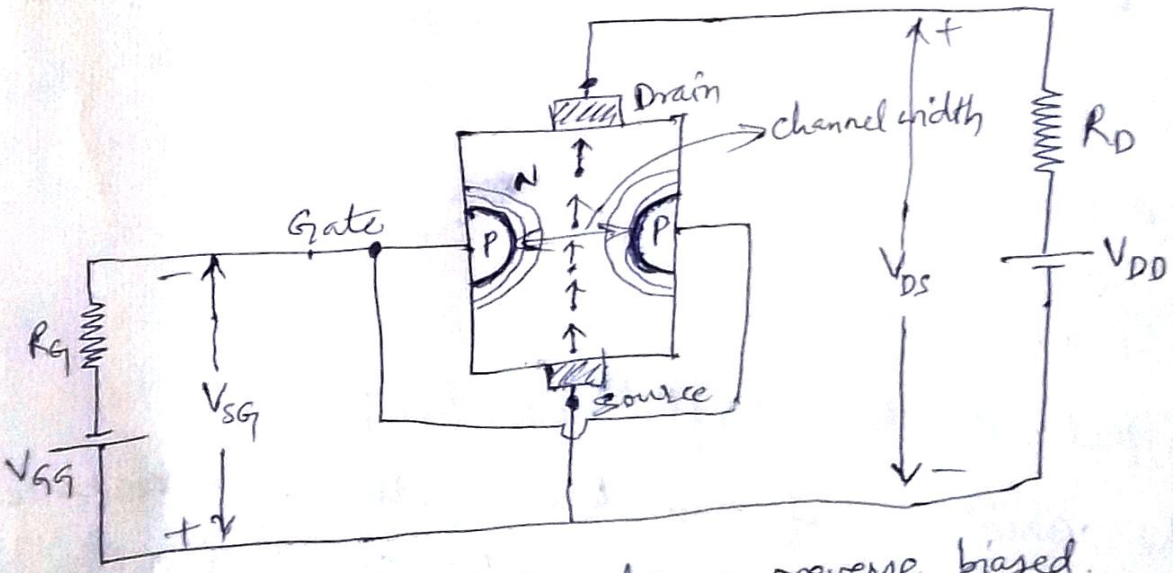
Field Effect transistor

FET is a unipolar, low-noise & voltage controlled device.



JFET:- Construction of N-channel JFET:-

JFET have 3 terminals - source, drain & gate.



1. Gate - source is always reverse biased.
2. Drain is always higher potential than source.

V_{DS} is always positive.
I_D value depends on V_{DS}
V_{GS} is always negative.

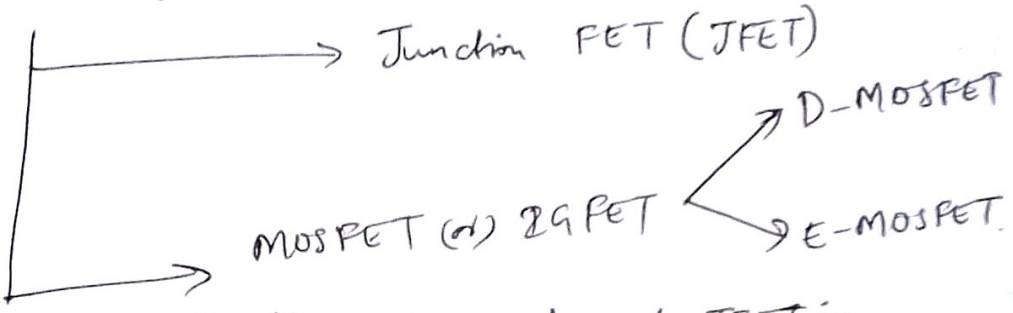
$I_D = f[V_{DS}]$

FET is voltage controlled device.

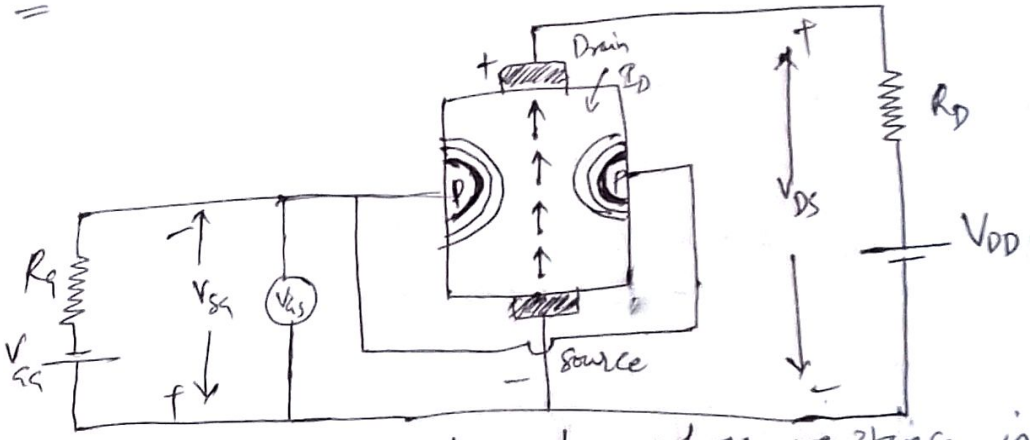
⊛ FET characteristics :-

FET is a unipolar, low noise & voltage controlled device.

⊛ Depending on the construction principle the FET are classified into



JFET :- Construction & Operation of N-channel JFET :-



First select the N type bar whose resistance is exactly divided 2 heavily doped p-type semiconductor are exactly diffused into N-type silicon bar.

The gap b/w two depletion regions are called channel width

JFET have 3 terminals source, gate & drain.

To make conduction of current the N-channel JFET must be properly biased.

i.e. (1) Gate-source is always reverse biased
(2) Drain-source higher potential than source.

V_{DS} is always (+)ve.

As $V_{DS} \uparrow$ $I_D \uparrow$

$V_{DS} \uparrow\uparrow$ $I_D \uparrow\uparrow$

* I_D value depends on V_{DS}. $\boxed{I_D = f(V_{DS})}$

→ V_{GS} is always negative values.

As $V_{GS} \uparrow$ – Depletion region widths ↑, channel width ↓ I_D ↓

As $V_{GS} \uparrow\uparrow$ $I_D \downarrow\downarrow$ $\boxed{I_D = f[V_{GS}]}$

$$I_D = f(V_{GS}, V_{DS})$$

→ Voltage controlled device.

$$I_D = f[V_{GS}, V_{DS}]$$

I_D vs V_{DS} when V_{GS} = constant

– Drain characteristics

I_D vs V_{GS} when V_{DS} = constant

– Transfer characteristics

⊛ JFET parameters:-

(i) Drain resistance (r_d)

$$\boxed{r_d = \frac{\Delta V_{DS}}{\Delta I_D}}$$

(ii) Transconductance (g_m)

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}}$$

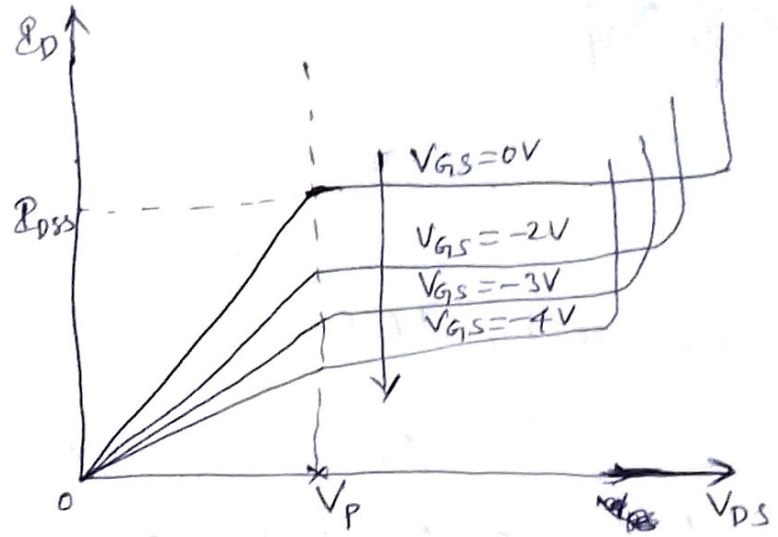
(iii) Amplification factor

$$\boxed{\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}}$$

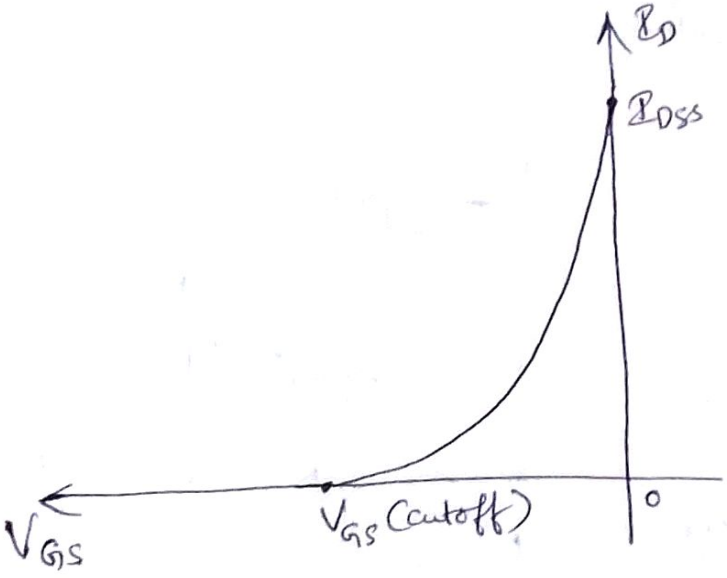
$$\boxed{\mu = g_m \times r_d}$$

⊛ V-I characteristics :-

Drain characteristics :- I_D vs V_{DS} when V_{GS} = Constant



Transfer characteristics :- I_D vs V_{GS} when V_{DS} = Constant



⊛ JFET parameters :-

(i) Drain Resistance (r_d) :-

$$r_d = \left[\frac{\Delta V_{DS}}{\Delta I_D}\right]$$

(ii) Transconductance (g_m) :-

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) \text{ (or) } \frac{dI_D}{dV_{GS}}$$

(iii) Amplification factor :-

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)$$

(*) MOSFET :-

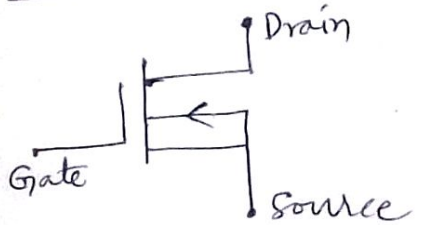
↳ Metal oxide semiconductor FET.

Depletion MOSFET

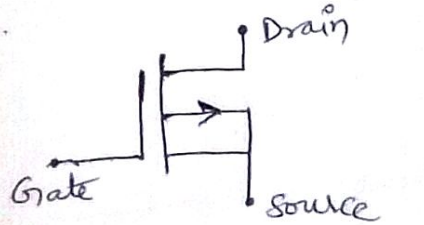
→ The channel exists b/w 'S' & 'D' terminals.

There is no necessity to apply a particular voltage b/w 'G' & 'S'.

→ Symbols (Representation)



N-channel D-MOSFET



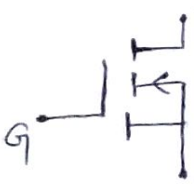
P-channel D-MOSFET

→ we can apply any potentials b/w 'G' & 'S' (positive, zero (or) negative)

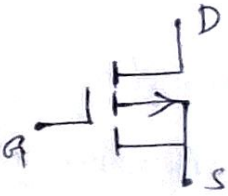
Enhancement MOSFET

→ No channel exists b/w 'S' & 'D' terminals.

→ Symbols (Representation)



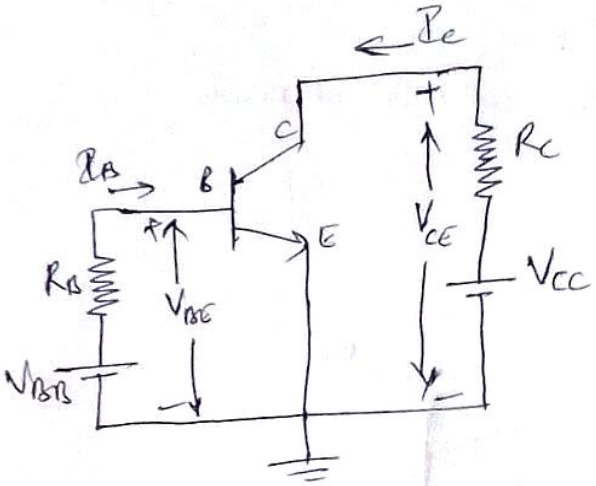
N-channel E-MOSFET



P-channel E-MOSFET

→ for N-channel E-MOSFET, V_{GS} is always positive

✱ TRANSISTOR BIASING



Apply KVL to i/p loop,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$I_B = \left(\frac{V_{BB} - V_{BE}}{R_B}\right)$$

Apply KVL to o/p loop,

$$V_{CC} - I_c R_c - V_{CE} = 0$$

$$I_c = \frac{V_{CC} - V_{CE}}{R_c}$$

$$V_{CE} = V_{CC} - I_c R_c$$

✱ On x-axis - Y-axis component is '0'

$(I_c = 0)$

$V_{CE} = V_{CC}$ → Max o/p voltage

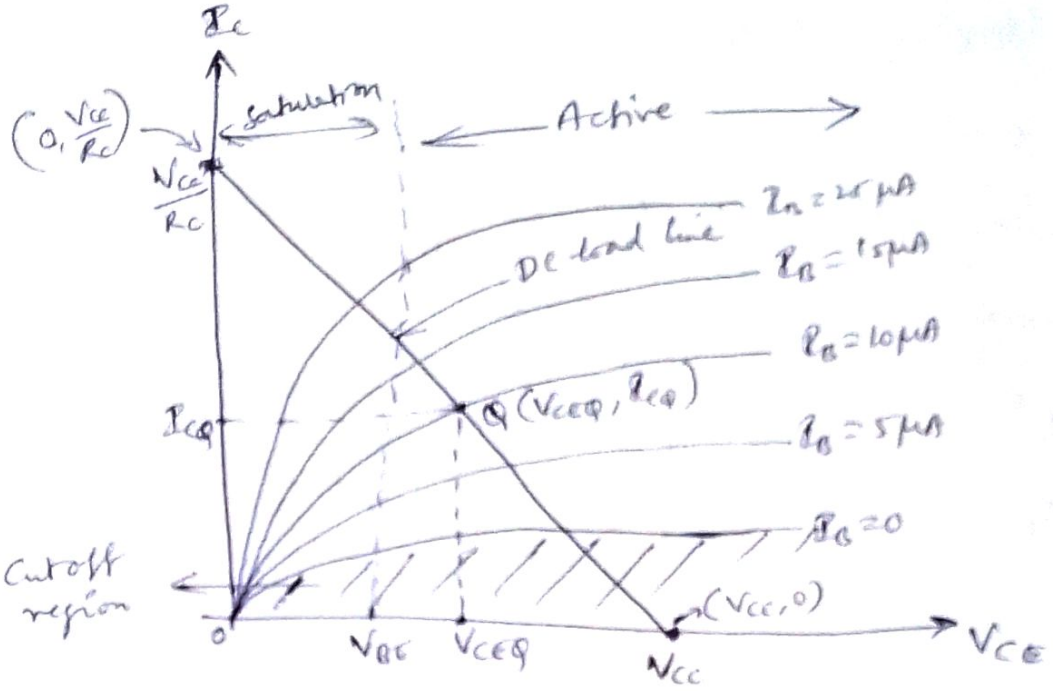
✱ On Y-axis - X-axis component is '0'

$(V_{CE} = 0)$

$$I_c = \frac{V_{CC} - V_{CE}}{R_{CC}} \quad (V_{CE} \to 0)$$

$$= \frac{V_{CC}}{R_c}$$

$I_c = \frac{V_{CC}}{R_c}$ → Max o/p current.



The line joining the cutoff point and the saturation point is called DC load line.

The point of intersection of DC load line and the transistor characteristics curve ~~and the DC load~~ is called operating point (or) Q point.

To do the faithful amplification, the operating point must be in the middle of the DC load line (or) near about the middle of the DC load line.

$Q(V_{CE}, I_C)$

$$I_C = \beta I_B + (1+\beta) I_O$$

Due to collection of charged particles by 'c'

temp. across the junction $I_C \uparrow$

As Temp. $\uparrow \Rightarrow I_O$, β & V_{BE} varies.

Effect of temp on I_o, β & V_{BE} :-

(i) As T↑ I_o↑

For every 1°C↑ temp. I_o↑ by 7%.

For every 10°C↑ " I_o doubles

$T_1°C \rightarrow I_{o_1}$ } $I_{o_2} = I_{o_1} \cdot 2^{\left(\frac{T_2 - T_1}{10}\right)}$

$T_2°C \rightarrow I_{o_2}$ }

(ii) As T↑ β↑

For 50°C↑ temp. β value of Ge transistor doubles

For 100°C↑ temp. β value of Si transistor doubles

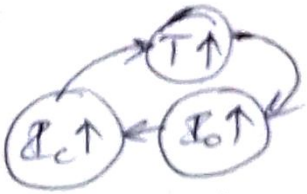
(iii) As T↑ V_{BE}↓

For 1°C↑ temp. V_{BE}↓ by 2.5mV.

I_C is effected more by I_o.

$$\boxed{I_C = f[I_o, V_{BE}, \beta]}$$

(*) As T↑ ⇒ I_o↑ ⟶ As I_o↑ ⇒ I_C↑ ⟶ As I_C↑ ⇒ T↑



Due to the collection of charged particles by the collector, temp. across the junction T_C increases. It becomes accumulative process At some particular state, temp. across the junction becomes maximum and breakdown of the collector junction takes place. this process is called "Thermal Runaway".

This is due to instability in the transistor simply the self destruction of it is called thermal runaway. To avoid this, the transistor must be stabilized.

Stabilization :-

I_o, V_{BE} & β due to temp.

The process of making the operating point independent of the variation in I_o, V_{BE}, β due to temp. is termed as stabilization.

The process of keeping the operating point in the active region is termed as stabilization.

The stability of a transistor is measured in stability factor.

Stability factor:-

$$I_c = f[V_{BE}, I_o, \beta]$$

$$\Delta I_c = \left\{\begin{matrix}\text{Change in } I_c \text{ due} \\ \text{to } I_o \text{ alone}\end{matrix}\right\} + \left\{\begin{matrix}\text{Change in } I_c \text{ due} \\ \text{to } V_{BE} \text{ alone}\end{matrix}\right\} + \left\{\begin{matrix}\text{Change in } I_c \\ \text{due} \\ \text{to } \beta \text{ alone}\end{matrix}\right\}$$

$$\Delta I_c = \left(\frac{\Delta I_c}{\Delta I_o} \times \Delta I_o\right)\Big|_{\substack{V_{BE}, \beta \\ = \text{Constant}}} + \left(\frac{\Delta I_c}{\Delta V_{BE}} \times \Delta V_{BE}\right)\Big|_{\substack{I_o, \beta \\ = \text{Constant}}} + \left(\frac{\Delta I_c}{\Delta \beta} * \Delta \beta\right)\Big|_{\substack{I_o, V_c \\ = \text{constant}}}$$

$$\Delta I_c = \frac{\Delta I_c}{\Delta I_o}\Big|_{\substack{V_{BE}, \beta \\ \text{Constant}}} \times \Delta I_o + \frac{\Delta I_c}{\Delta V_{BE}}\Big|_{\substack{I_o, \beta \\ \text{Constant}}} \Delta V_{BE} + \frac{\Delta I_c}{\Delta \beta}\Big|_{\substack{I_o, V_{BE} \\ \text{Constant}}} \Delta \beta$$

$$\Delta I_c = S \Delta I_o + S' \Delta V_{BE} + S'' \Delta \beta$$

where $S = \left.\frac{\Delta I_c}{\Delta I_o}\right|_{V_{BE}, \beta = \text{constant}}$

$S' = \left.\frac{\Delta I_c}{\Delta V_{BE}}\right|_{I_o, \beta = \text{constant}}$

$S'' = \left.\frac{\Delta I_c}{\Delta \beta}\right|_{I_o, V_{BE} = \text{constant}}$

} Stability factor

Stability factor (S)

$$S = \frac{\Delta I_c}{\Delta I_o} \text{ (or) } \left.\frac{dI_c}{dI_o}\right|_{V_{BE}, \beta = \text{constant}}$$

$$I_c = \beta I_B + (1+\beta) I_o$$

Differentiate w.r.t. I_c.

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{dI_o}{dI_c}$$

$$1 - \beta \frac{dI_B}{dI_c} = (1+\beta) \frac{1}{S}.$$

$$\boxed{S = \frac{(1+\beta)}{1 - \beta \frac{dI_B}{dI_c}}}$$

To calculate $\frac{dI_B}{dI_c}$,

(i) always take i/p loop equations of the given transistor ckt.

(ii) Differentiate w.r.t. I_c, we get $\left(\frac{dI_B}{dI_c}\right)$ value.

(iii) If $S \to$ very high (or) high $\Rightarrow S = \frac{\Delta I_c}{\Delta I_o} \to$ The ckt. is thermally less stable.

If $S \to$ low $\Rightarrow$ The ckt. is thermally more stable.

⊛ Biasing Methods:-

The biasing methods are used to keep the operating point in the active region.

The Biasing methods are:

1. Fixed Bias Method.
2. Collector-to-Base bias.

   (OR)

   Feedback Resistor bias.
3. Voltage Divider bias

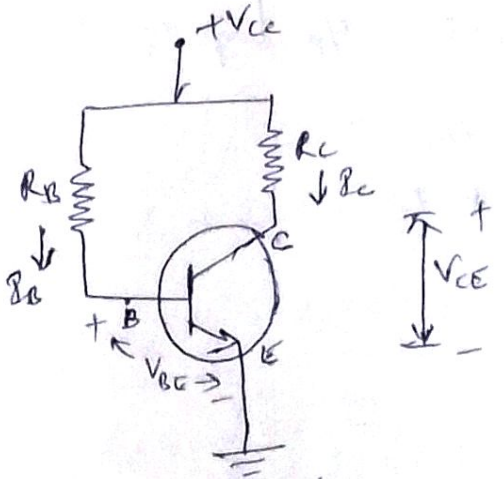
   (OR)

   Emitter bias

   (OR)

   Self bias method.

(1) Fixed Bias method:-



Apply KVL to i/p loop:-

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$-I_B = \frac{V_{BE} - V_{CC}}{R_B} \Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

$\boxed{I_C = \beta I_B}$ → Assuming the transistor operated in active region.

Feedback Resistor Bias Method:-

Apply KVL to o/p Loop:-

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

Note:-

If the estimated V_{CE} voltage satisfies the condition

$$\boxed{V_{CE(sat)} < V_{CE} < V_{CC}}$$

→ Transistor operating in active region

$$V_{BE} = V_\gamma \rightarrow \begin{cases} J_E \rightarrow F.B. \\ J_C - R.B \end{cases} \text{ Active region.}$$

Else the transistor operates in saturation region.

If it is in this region,

$$-V_{CE} = V_{CE(sat)} = \begin{cases} 0.2V \rightarrow Si \\ 0.1V \rightarrow Ge. \end{cases}$$

Stability Factor

To calculate 'S' take i/p loop equations

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Differentiate w.r.t I_C

$$0 - \frac{dI_B}{dI_C} \times R_B - 0 = 0$$

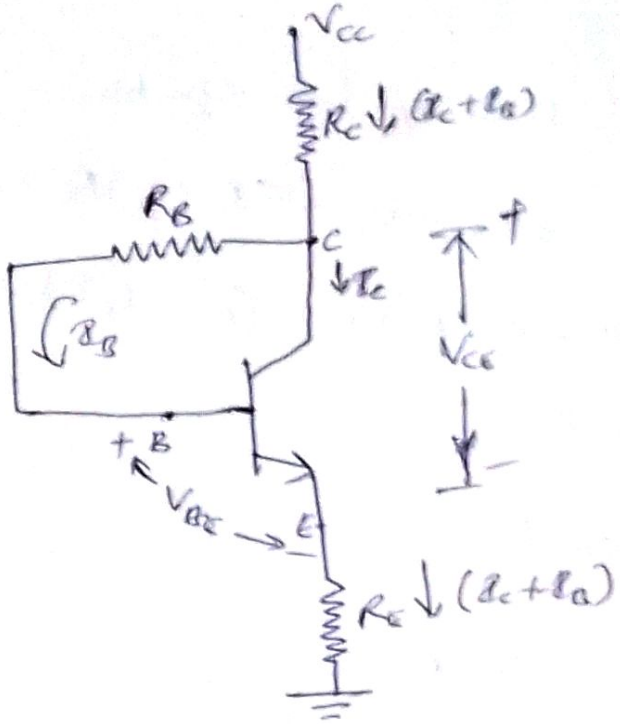
$$\therefore \frac{dI_B}{dI_C} = 0$$

$$\boxed{S = (1+\beta)}$$

$\beta \rightarrow$ high
$S \rightarrow$ high

The fixed bias ckt. is thermally less stable.

(2) Collector-to-Base bias or) Feedback Resistor Bias Method:



Apply KVL to i/p loop

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - (I_C + I_B)R_E = 0$$

Assume that the transistor is operating in the active region, we get:

$$\boxed{I_C = \beta I_B}$$

$$I_C + I_B = (1+\beta) I_B$$

$$V_{CC} - (1+\beta) I_B \cdot R_C - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}}$$

$$\boxed{I_C = \beta I_B}$$

Apply KVL to o/p loop,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} - (I_C + I_B)R_E = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B)(R_C + R_E)$$

Stability factor (S):-

To calculate 'S' take i/p loop equation.

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - (I_C + I_B)R_E = 0$$

$$V_{CC} - V_{BE} - (R_C + R_B + R_E)I_B - (R_C + R_E)I_C = 0$$

Differentiate w.r.t. I_C.

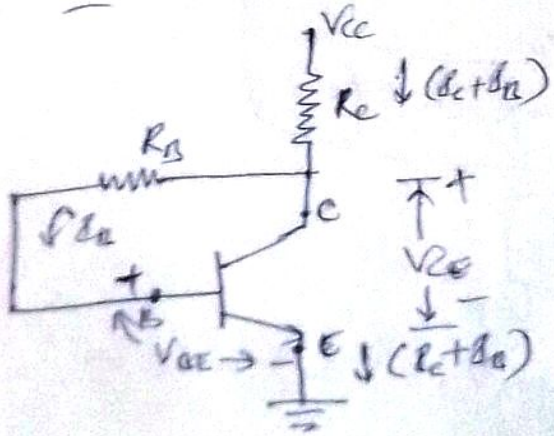
$$0 - 0 - (R_C + R_B + R_E)\frac{dI_B}{dI_C} - (R_C + R_E) = 0$$

$$\frac{dI_B}{dI_C} = -\left[\frac{R_C + R_E}{R_C + R_B + R_E}\right]$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C + R_E}{R_C + R_B + R_E}\right)}$$

$$S = \frac{(1+\beta)}{1+\beta\left[\frac{(I_C + I_B)\text{ current flowing resistors sum}}{I_B\text{ current flowing resistor sum}}\right]}$$

Without 'R_E' :-



Put $R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}$$

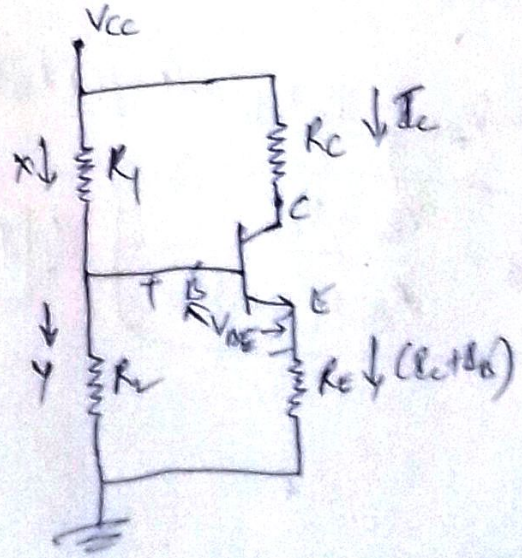
Note: (2) Collector to base bias ckt. is thermally more stable compared to fixed bias ckt.

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} \cong 1+\beta \quad \text{if } R_C = 0$$

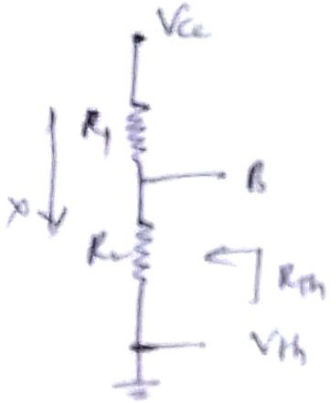
The ckt. is thermally less stable

∴ The collector to base bias method 'R_C' value should not be very small.

(3) Voltage divider (or) Emitter (or) Self bias method:-



Thevenin's Equivalent ckt :-



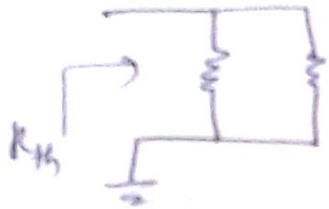
$V_{Th} = x R_2$

$x = \frac{V_{cc}}{R_1 + R_2}$

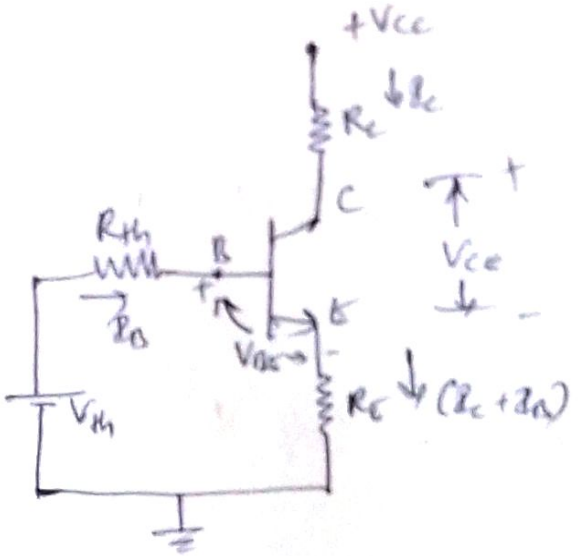
$V_{Th} = \frac{V_{cc}}{R_1 + R_2} \times R_2$

$$V_{Th} = V_{cc}\left(1 + \frac{R_2}{R_1}\right)$$

R_{Th} :-



$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$



Apply KVL to i/p loop :-

$V_{Th} - I_B R_{Th} - V_{BE} - (I_c + I_B) R_c = 0$

Assume that the transistor operates in the active region

$I_c = \beta I_B$ & $I_c + I_B = (1+\beta) I_B$

$\Rightarrow V_{Th} - V_{BE} - I_B R_{Th} - (1+\beta) I_B R_c = 0$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_c}$$ & $$I_c = \beta I_B$$

Apply KVL to o/p loop :-

$$V_{CC} - I_C R_C - V_{CE} - R_E (I_C + I_B) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E}$$

Stability factor :-

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{Th}+R_E}\right)}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{1}{\frac{R_{Th}}{R_E}+1}\right)}}$$

if $\frac{R_{Th}}{R_E} \to \infty \Rightarrow S \to (1+\beta)$

$\therefore$ The ckt. is thermally less stable

if $\frac{R_{Th}}{R_E} \to 0 \Rightarrow S \to 1 \Rightarrow$ The ckt. is thermally more stable.

But $S \simeq 1 \to$ practically not possible.

For $S = 1$:- $\frac{R_{Th}}{R_E} = 0$

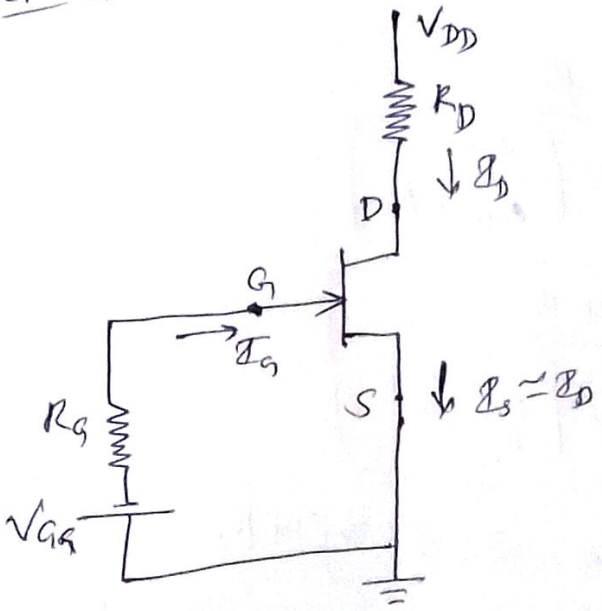
i.e. $R_{Th} = 0$, $R_E = 0 \to$ Collector $\to$ O.C $\to$ (Transistor OFF)

$R_{Th} = 0$ $\begin{cases} R_1 = 0 \to V_B > V_C \to J_C \to F.B. \text{ (saturation region)} \\ R_2 = 0 \to J_E \to R.B. \to \text{(cutoff region)} \end{cases}$

⊛ FET Biasing :-

Methods
- → Fixed bias
- → Self bias
- → Voltage divider bias

① fixed bias Method :-



$\{ I_{DSS}, V_{GS(off)} \}$

$I_D >> I_G \Rightarrow \boxed{I_G \simeq 0}$

$I_G R_G = 0 \; ; \; V_G \simeq -V_{GS}$

$V_S = 0$

$V_{GS} = V_{GS} - V_S$

$= -V_{GG}$

⊛ ⇒ Substitute V_{GS} in I_D equation

we get $I_D \simeq I_S$

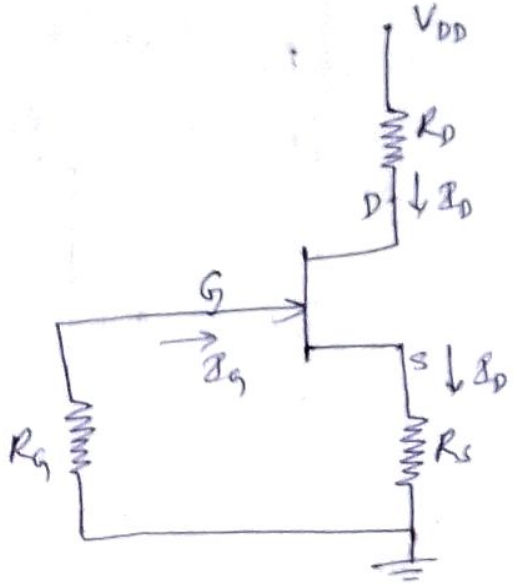
$Q_{pt.}(V_{GS}, I_D)$

↓

Q-Point

② Self bias Method :-

There is no necessity of Supply voltage 'V_{GG}'.



$I_G \simeq 0$

$I_G R_G \simeq 0$

$V_G \simeq 0\,V$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

Substitute V_{GS} value in I_D equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]^2$$

$$= I_{DSS}\left[1 - \left(\frac{-I_D R_S}{V_{GS(cutoff)}}\right)\right]^2$$

By simplifying we get a quadratic equation

By solving ⇒ we get $\{I_{D_1}, I_{D_2}\}$

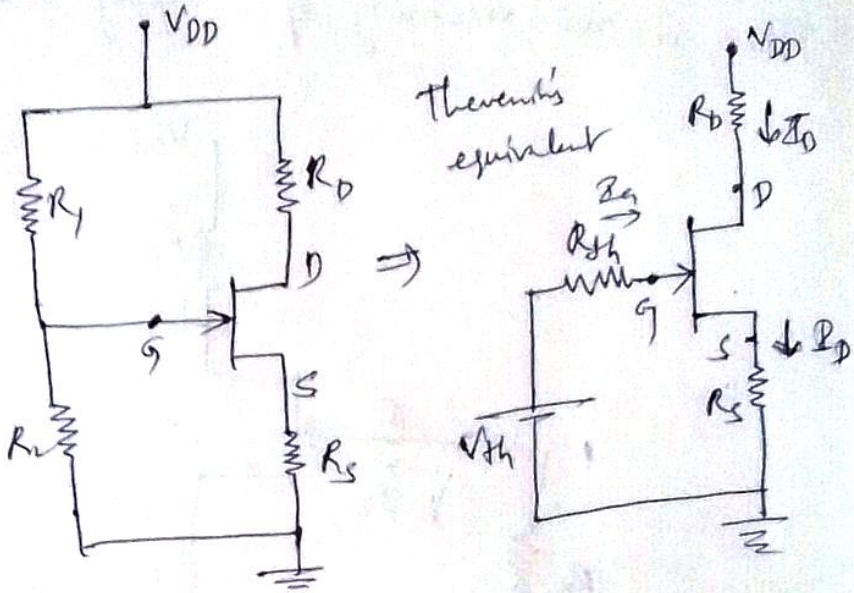
→ Choose the correct value of I_D

↓

Note:-

Always choose the lower value of I_D.

③ Voltage divider bias :-



$$V_{Th} = V_{DD}\left(\frac{R_2}{R_1+R_2}\right)$$

$$R_{Th} = \frac{R_1 R_2}{R_1+R_2}$$

$I_G \simeq 0$

$I_G R_{Th} \simeq 0$

$V_G \simeq V_{Th}$

$$\boxed{V_S \simeq I_D R_S}$$

$V_{GS} = V_G - V_S$

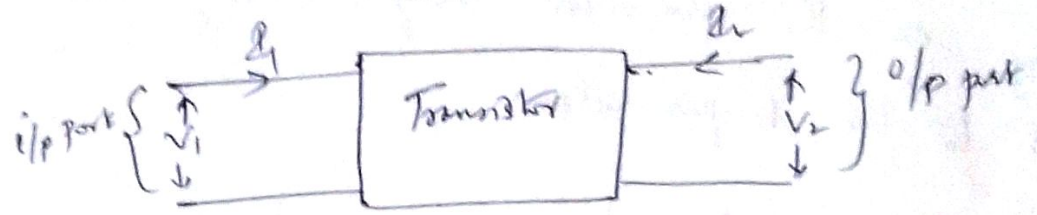
$$\boxed{V_{GS} = V_{Th} - I_D R_S}$$

Substitute V_{GS} value in I_D equation, we get a quadratic equation.

By solving we get $\{ I_{D_1}, I_{D_2} \}$

Choose the correct value of drain current.

⊛ AMPLIFIERS [TRANSISTOR AMPLIFIERS]



Inputs (V_1, I_1)

Outputs (V_2, I_2)

For a BJT transistor, dependents (V_1, I_2)

Independents (I_1, V_2)

In general, we express this relationship as,

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$
} h-parameter equations of transistor

When $V_2 = 0$ i.e. o/p port S.C :-

$$V_1 = h_{11} I_1, \quad I_2 = h_{21} I_1$$

$$h_{11} = \left(\frac{V_1}{I_1}\right) \rightarrow \text{input impedance } h_i (\Omega).$$

$$h_{21} = \left(\frac{I_2}{I_1}\right) \rightarrow \text{forward current gain } (h_f).$$

When $I_1 = 0$ i.e. i/p port O.C :-

$$V_1 = h_{12} V_2 ; \quad I_2 = h_{22} V_2$$

$$h_{12} = \left[\frac{V_1}{V_2}\right] \rightarrow \text{Reverse voltage gain } (h_r)$$

$$h_{22} = \left[\frac{I_2}{V_2}\right] \rightarrow \text{o/p admittance } h_o (\mho)$$

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

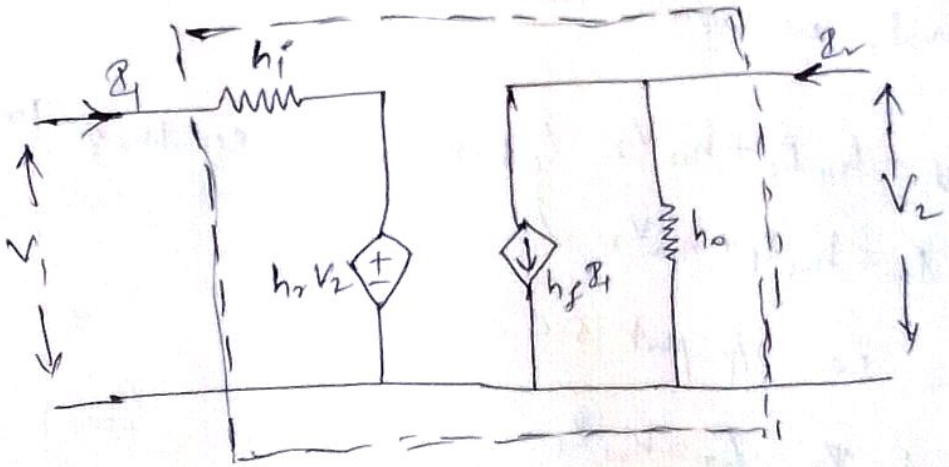
Depending on the transistor configuration, add a sub-script to the h-parameters.

CB → $h_{ib}, h_{rb}, h_{fb}, h_{ob}$

CE → $h_{ie}, h_{re}, h_{fe}, h_{oe}$

CC → $h_{ic}, h_{rc}, h_{fc}, h_{oc}$.

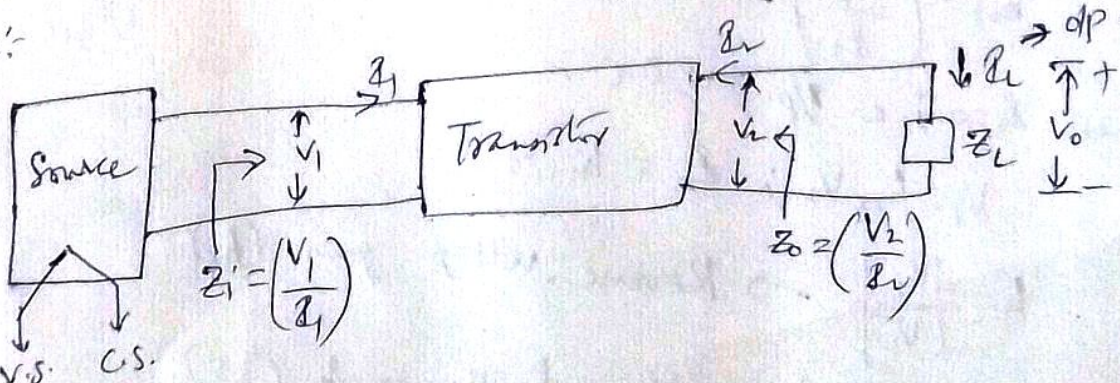
The small signal model (or) equivalent ckt. of a transistor :-



$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

Amplifier Analysis :-



Analysis includes the calculation of the following:

(1) Current gain, $A_I = \left(\frac{I_L}{I_1}\right)$

(2) Input impedance, $Z_i = \left(\frac{V_1}{I_1}\right)$

(3) Voltage gain, $A_V = \left(\frac{V_0}{V_1}\right)$

(4) o/p impedance, $Z_0 = \left(\frac{V_2}{I_2}\right)$

(5) Voltage amplification (or) Overall voltage gain } $\boxed{A_{VS} = \left(\frac{V_0}{V_S}\right)}$

(6) Current Amplification (or) Overall current gain } $\boxed{A_{IS} = \left(\frac{I_L}{I_S}\right)}$

$$\left.\begin{aligned} V_1 &= h_i I_1 + h_r V_2 \\ I_2 &= h_f I_1 + h_o V_2 \end{aligned}\right\}$$ Use these equations.

(1) Current gain :- (A_I)

$$A_I = \frac{I_L}{I_1} = \frac{-I_L}{I_1}$$

$$I_L = h_f I_1 + h_o V_2$$

But $V_2 = V_0 = I_L Z_L = -I_L Z_L$

$$I_2 = h_f I_1 + h_o(-I_L Z_L)$$

$$I_2(1 + h_o Z_L) = h_f I_1$$

$$\left(\frac{I_2}{I_1}\right) = \frac{h_f}{(1+h_o Z_L)}$$

$$\boxed{A_I = \frac{-I_2}{I_1} = \frac{-h_f}{(1+h_o Z_L)}}$$

② I/p impedance:-

$$Z_i = \frac{V_1}{I_1} \qquad (\text{or}) \qquad Z_i = h_i + h_r\left[\frac{-h_f}{1+h_o Z_L}\right] Z_L$$

$$V_1 = h_i I_1 + h_r V_2$$

$$V_1 = h_i I_1 + h_r(-I_2 Z_L)$$

$$= I_1\left(h_i + h_r\left(\frac{-I_2}{I_1}\right) Z_L\right)$$

$$\therefore \boxed{Z_i = \frac{V_1}{I_1} = h_i + h_r A_I Z_L}$$

$$= h_i - \frac{h_o h_f}{1+h_o Z_L} \times Z_L$$

$$= h_i - \frac{h_r h_f}{\left(\frac{1+h_o Z_L}{Z_L}\right)}$$

$$\boxed{Z_i = h_i - \frac{h_r h_f}{\left(\frac{1}{Z_L} + h_o\right)}}$$

③ Voltage gain:-

$$A_V = \frac{V_o}{V_1} = \frac{V_2}{V_1}$$

$$A_V = \left(\frac{-I_2 Z_L}{V_1}\right)$$

$$\frac{V_1}{I_1} = Z_i \Rightarrow V_1 = Z_i I_1$$

$$A_V = \frac{-I_2 Z_L}{Z_i I_1} = \left(\frac{-I_2}{I_1}\right)\cdot\frac{Z_L}{Z_i}$$

$$\boxed{A_V = \frac{A_I Z_L}{Z_i}}$$

④ o/p impedance :-

$$Z_o = \left(\frac{V_2}{I_2}\right) \Bigg|_{\substack{\text{load} \to \text{o.c.} \\ \text{All the sources set equal to zero.}}}$$

$$I_2 = h_f I_1 + h_o V_2$$

$$= V_2\left[h_o + h_f \frac{I_1}{V_2}\right]$$

$$\frac{I_2}{V_2} = \frac{1}{Z_o} = Y_o = h_o + h_f\left[\frac{I_1}{V_2}\right]$$

To calculate Z_o, first calculate $\left(\frac{I_1}{V_2}\right)$

Apply KVL to i/p loop,

$$0 - I_1(R_s + h_i) - h_r V_2 = 0$$

$$\boxed{\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}}$$

$$Y_o = h_o + h_f\left[\frac{-h_r}{R_s + h_i}\right]$$

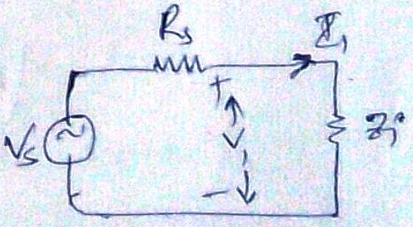
$$\boxed{Y_o = h_o - \frac{h_r h_f}{R_s + h_i}}$$

⑤ voltage amplification :-

$$A_{VS} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_i}\right)\left(\frac{V_i}{V_s}\right)$$

$$A_{VS} = A_V\left(\frac{V_i}{V_s}\right)$$

$$V_i = V_s\left(\frac{Z_i}{R_s + Z_i}\right)$$



$$A_{VS} = A_V \left[\frac{Z_i}{R_S + Z_i}\right]$$

$\frac{Z_i}{R_S+Z_i} < 1$

$$\boxed{A_{VS} < A_V}$$

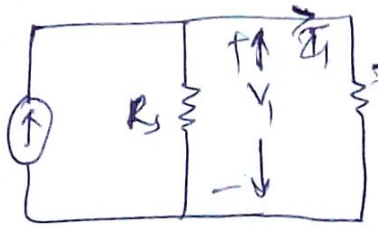
For an ideal voltage source, $R_S = 0$

$$\boxed{A_{VS} = A_V}$$

(6) Current Amplification :-

$$A_{IS} = \left(\frac{I_L}{I_S}\right) = \left[\frac{I_L}{I_i}\right]\left[\frac{I_i}{I_S}\right]$$

$$\Rightarrow A_{IS} = A_I \left(\frac{I_i}{I_S}\right)$$



$$\Rightarrow I_i = I_S \left(\frac{R_S}{R_S + Z_i}\right)$$

$$\boxed{\therefore A_{IS} = A_I \left(\frac{R_S}{R_S + Z_i}\right)}$$

$$\Rightarrow A_{IS} < A_I$$

For an ideal current source, $R_S = \infty$

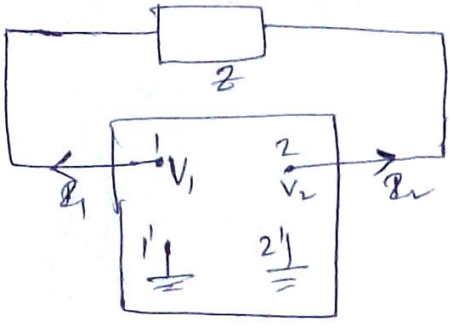
$$A_{IS} = A_I \left[\frac{1}{1 + \frac{Z_i}{R_S}}\right]$$

$\frac{Z_i}{R_S} \to 0$

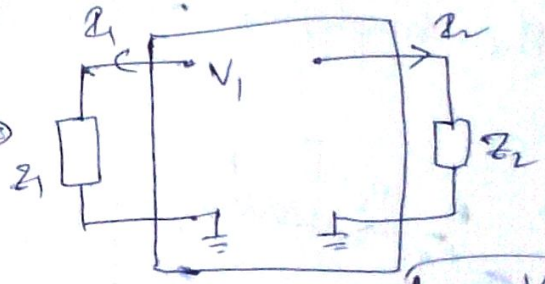
$$\boxed{A_{IS} = A_I}$$

⊛ Miller's theorem:-

In a linear circuit, if there exists a branch with impedance Z, connecting two nodes with nodal voltages V_1 and V_2, we can replace this branch by two branches connecting the corresponding nodes to ground by impedances respectively $\frac{Z}{(1-A_V)}$ & $\frac{ZA_V}{(A_V-1)}$



$\Rightarrow$



$$I_1 = \frac{V_1 - V_2}{Z}$$

$$= \frac{1}{Z} V_1 \left(1 - \frac{V_2}{V_1}\right)$$

$$I_1 = \frac{1}{Z} V_1 (1 - A_V)$$

$$\frac{V_1}{I_1} = \frac{Z}{1-A_V} \Rightarrow \boxed{Z_1 = \frac{Z}{1-A_V}}$$

$$I_2 = \frac{V_2 - V_1}{Z} = \frac{1}{Z} V_2 \left(1 - \frac{V_1}{V_2}\right) = \frac{1}{Z} V_2 \left[1 - \frac{1}{A_V}\right]$$

$$\boxed{Z_2 = \frac{V_2}{I_2} = \frac{Z}{\left(1 - \frac{1}{A_V}\right)}} = \frac{ZA_V}{(A_V - 1)}$$

$I_1 = \frac{V_1}{Z_1}$ $\Rightarrow$ $\boxed{Z_1 = \frac{V_1}{I_1}}$

$\boxed{Z_2 = \frac{V_2}{I_2}}$

Its dual version is based on Kirchoff's current law

Dual of Millers theorem is also called Millers theorem for current.

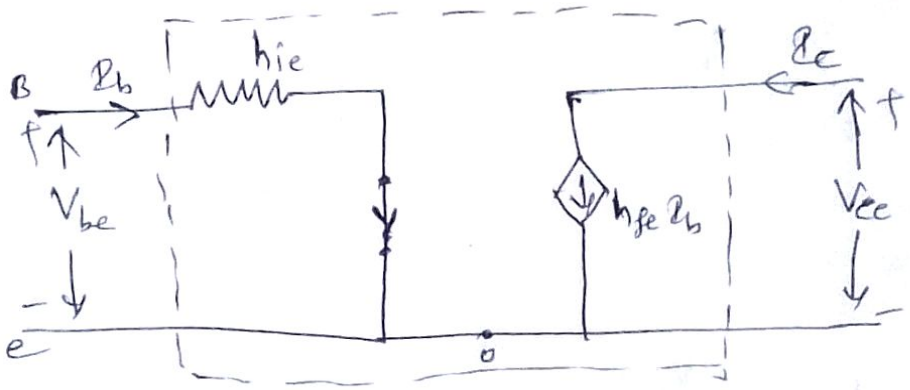
⊛ Simplified h-parameter model (or) Approximate model:-

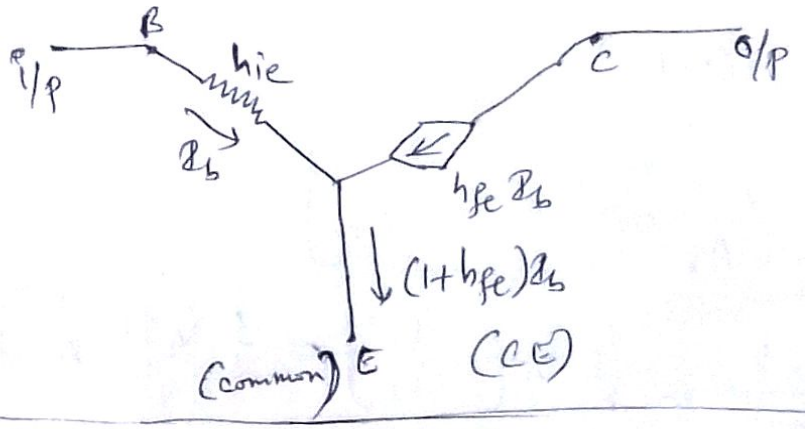
This model based on CE → we must use h-parameters of CE only i.e. ($h_{ie}, h_{re}, h_{fe}, h_{oe}$)

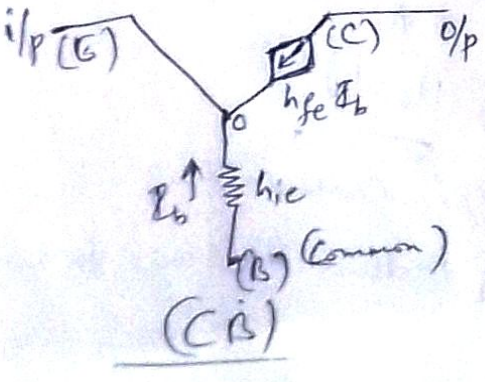
In simplified model we neglect $\begin{cases} h_{re}V_{ce} \\ h_{oe}V_{ce} \end{cases}$

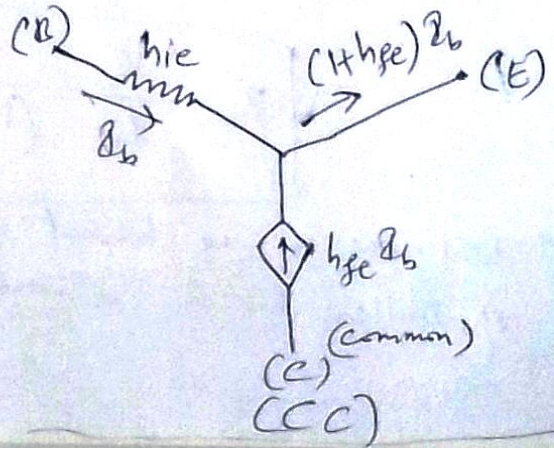
Reason for this is the current passing through $\left(\frac{1}{h_{oe}}\right)$ is very low ($\simeq 0$) $\left[\because \frac{1}{h_{oe}} \text{ is very high}\right]$

The simplified model of the transistor is









SINGLE STAGE AMPLIFIERS

Classification of Amplifiers:-

BJT Amplifiers
- → CE Amplifier
- → CB Amplifier
- → CC Amplifier

FET Amplifiers
- → CD Amplifier
- → CS Amplifier
- → CG Amplifier

Distortion in Amplifiers:-

Distortion is the alteration of the original shape (or other characteristic) of the waveform of a signal in an electronic device.

Types of distortion include:

Amplitude distortion:-

O/p amplitude is not a linear function of the i/p amplitude under specified conditions.

Frequency (or) Harmonic distortion:-

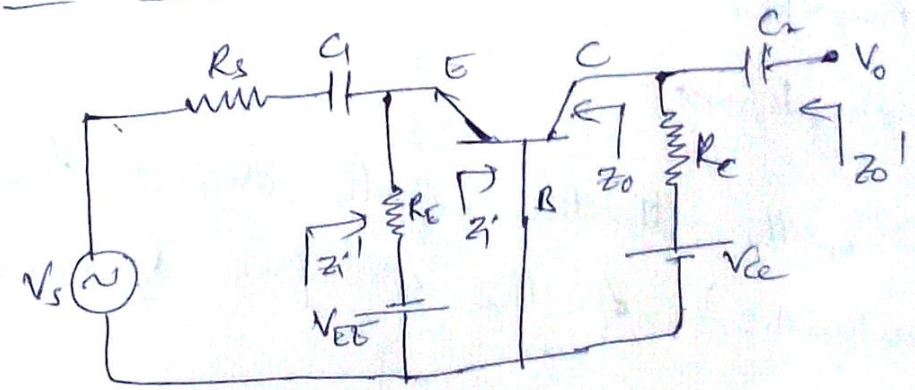
These distortions are overtones added to a pure sinewave fed to the system.

Phase distortion:-

This form of distortion occurs due to electrical reactance. Here all the components of the i/p signal are not amplified with the same phase shift, hence making some parts of the o/p signal out of phase with the rest of the o/p.

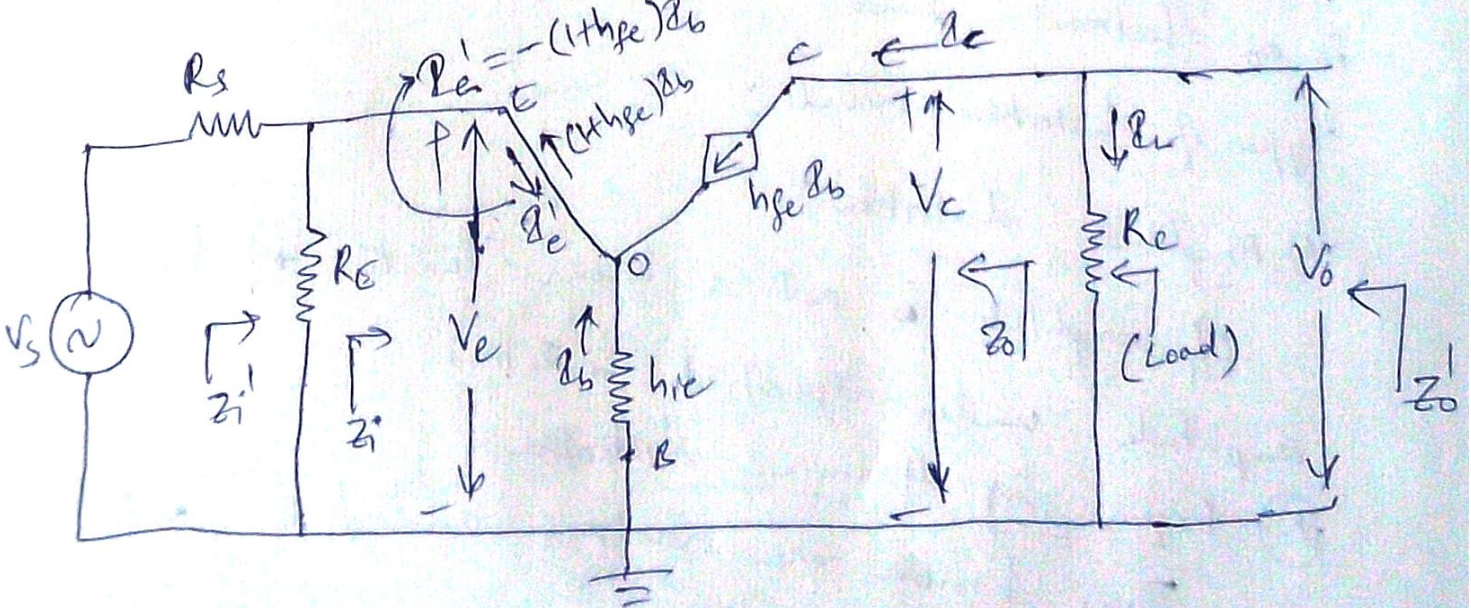
CE Amplifier (already discussed in previous module under hybrid parameters) (i) $Z_i = h_{ie}$ (ii) $Z_o = \infty$ (iii) $A_V = \frac{-h_{fe} R_c}{h_{ie}}$

CB Amplifier:-



$R_L = R_c$

$= -h_{fe} R_b$



① Current gain :-

$$A_I = \left(\frac{I_L}{I_e'}\right) = \frac{-h_{fe} I_b}{-(1+h_{fe}) I_b} = \frac{h_{fe}}{(1+h_{fe})}$$

As $D_r > N_r \Rightarrow \boxed{A_I < 1}$

But if $h_{fe} >>> 1 \Rightarrow A_I \simeq 1$

The o/p current ≃ i/p current

The ckt. is current follower (or) current Buffer.

∴ The CB Amplifier used as a current Buffer ckt.

② Input Impedance :-

$$Z_i = \frac{V_e}{I_e'}$$

$$V_e = -h_{ie} I_b \Rightarrow Z_i = \frac{-h_{ie} I_b}{-(1+h_{fe}) I_b} = \frac{h_{ie}}{(1+h_{fe})}$$

$$\therefore \boxed{Z_i' = \frac{h_{ie}}{1+h_{fe}}} \Rightarrow Z_i \text{ is very low}$$

$$Z_i' = Z_i // R_E$$

Voltage gain :-

$$A_V = \left(\frac{V_o}{V_e}\right)$$

$$V_o = I_L R_c = -h_{fe} I_b R_c$$

$$V_e = -h_{ie} I_b$$

$$\therefore A_V = \left(\frac{h_{fe} R_c}{h_{ie}}\right)$$

Voltage Amplification:-

$$A_{VS} = \left(\frac{V_o}{V_s}\right) = \left(\frac{V_o}{V_e}\right)\left(\frac{V_e}{V_s}\right)$$

$$\boxed{A_{VS} = A_V\left(\frac{V_e}{V_s}\right)}$$

$$V_e = V_s\left[\frac{Z_i'}{Z_i' + R_s}\right]$$

$$A_{VS} = A_V\left[\frac{\cancel{V_s}\left[\frac{Z_i'}{Z_i'+R_s}\right]}{\cancel{V_s}}\right]$$

$$\boxed{A_{VS} = A_V\left[\frac{Z_i'}{Z_i' + R_s}\right]}$$

As $R_s >>> Z_i'$

$$\Rightarrow A_{VS} <<< A_V$$

(A_{VS} is very low for CB Amplifier)

∴ The CB Amplifier cannot be used for voltage Amplification.

O/P Impedance (Z_o):-

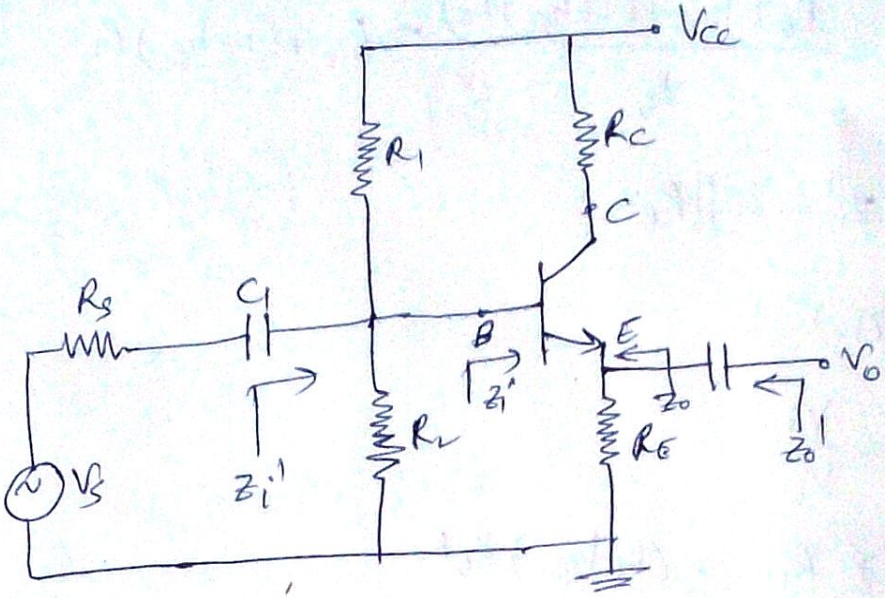
$$Z_o = \left(\frac{V_o}{I_o}\right) \Bigg|_{\substack{R_c \to O.C. \\ \& \\ V_s = 0}}$$

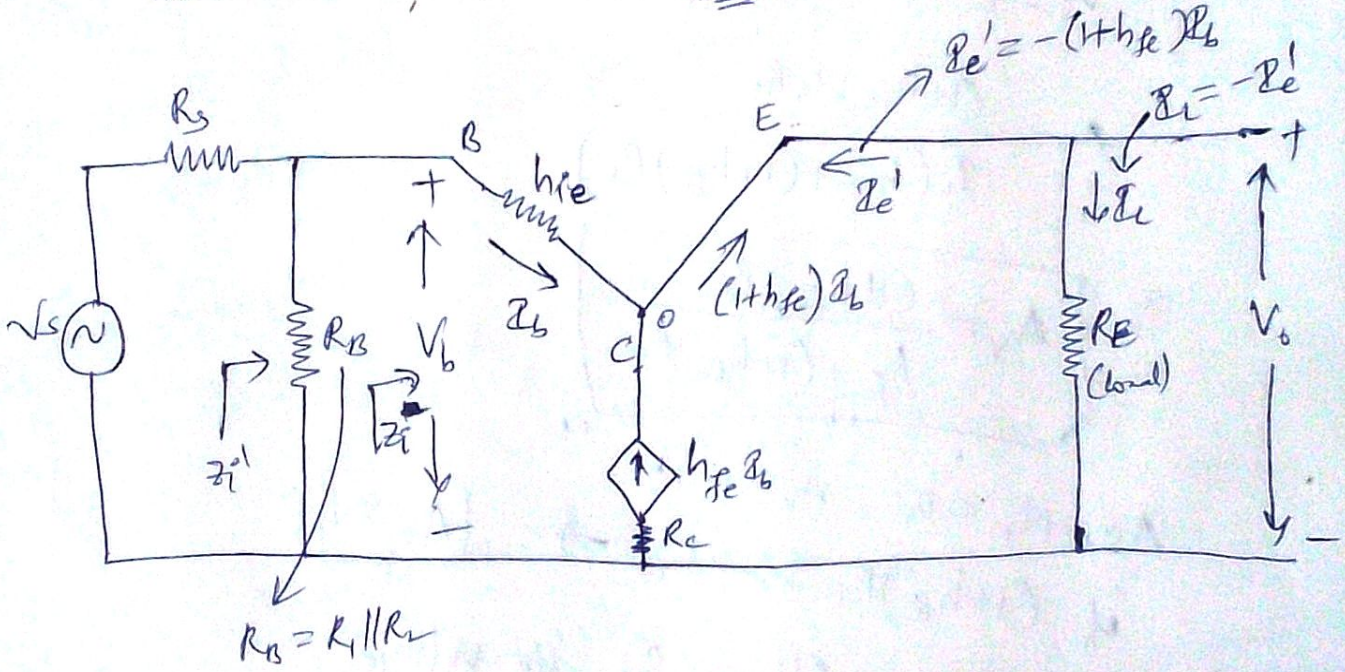
$$Z_o' = R_c \| Z_o$$

$$\because Z_o = \infty$$

$$Z_o' = R_c$$

⊛ CC Amplifier :-





Current gain :-

$$A_I = \frac{I_L}{I_b} = \frac{(1+h_{fe})I_b}{I_b} = (1+h_{fe})$$

Input impedance :-

$$Z_i = \left(\frac{V_b}{I_b}\right)$$

$$V_b = h_{ie} I_b + I_L R_E$$

$$= h_{ie} I_b + (1+h_{fe}) I_b R_E$$

$$V_b = I_b (h_{ie} + (1+h_{fe}) R_E)$$

$$Z_i = \frac{V_b}{I_b} = \frac{I_b (h_{ie} + (1+h_{fe}) R_E)}{I_b} = h_{ie} + (1+h_{fe}) R_E$$

$$Z_i' = Z_i \,||\, R_B$$

Voltage Gain (A_V) :-

$$A_V = \frac{V_o}{V_b}$$

$$V_o = I_e R_E = (1+h_{fe}) I_b R_E$$

$$A_V = \frac{(1+h_{fe}) I_b R_E}{I_b (h_{ie} + (1+h_{fe}) R_E)}$$

$$\boxed{A_V = \frac{(1+h_{fe}) R_E}{h_{ie} + (1+h_{fe}) R_E}}$$

As $N_r < D_r$; $A_V < 1$

if $(1+h_{fe}) R_E >> h_{ie} \Rightarrow \therefore \boxed{A_V \simeq 1}$

The O/p voltage follows the i/p voltage.

- Voltage follower circuit
  (or)
- Voltage Buffer circuit
  (or)
- Emitter follower circuit.

CC Amplifier is used as voltage buffer circuit

Voltage Amplification :-

$$A_{VS} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_b}\right)\left(\frac{V_b}{V_s}\right) = A_V\left(\frac{V_b}{V_s}\right)$$

$$V_b = V_s\left[\frac{Z_i'}{Z_i' + R_s}\right]$$

$$A_{VS} = A_V\left(\frac{V_b}{V_s}\right) = A_V\left[\frac{Z_i'}{Z_i' + R_s}\right]$$

As $A_V < 1$; $A_{VS} < 1$

∴ CC Amplifier cannot be used for voltage amplification

O/P impedance (Z_o) :-

$$Z_o = \frac{V_e}{I_e'} \Bigg| \begin{array}{c} R_E \to \text{O.C.} \\ \& \\ V_s = 0. \end{array}$$

$$V_e = -I_b(h_{ie} + R_s')$$

$$I_e' = -(1 + h_{fe}) I_b$$

$$\therefore Z_o = \frac{I_b(h_{ie} + R_s')}{(1 + h_{fe}) I_b}$$

$Z_o \to$ very low for CC Amplifier $\Rightarrow$ $\boxed{Z_o = \dfrac{h_{ie} + R_s'}{1 + h_{fe}}}$

$$\boxed{Z_o' = Z_o \| R_E}$$

Note :- FET Amplifiers (CD, CS & CG) were already discussed during biasing in previous modules.

Amplifier Analysis

With Resistive load: (preference of amplifier is also important)

→ Among the three amplifiers CE is only used for amplification.

→ For CE Amplifier

(i) $Z_i = h_{ie}$ ⟶ very low

(ii) $Z_o = \infty$ ⟶ very high

(iii) $A_v = \frac{-h_{fe} R_c}{h_{ie}}$ ⟶ very high.

The expected values from the amplifier are

(i) A_v → very high — (more amplification)

(ii) Z_i → very high — ↑ driving capacity of circuit

(iii) Z_o → very low — ↓ the loading effect on i/p signal.

To increase thermal stability & to improve the impedance characteristics negative feedback is usually employed.